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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,963	03/23/2004	Steven C. Goss	TI-36791	2345

23494 7590 10/24/2007  
TEXAS INSTRUMENTS INCORPORATED  
P O BOX 655474, M/S 3999  
DALLAS, TX 75265

EXAMINER
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POWERS, WILLIAM S

ART UNIT	PAPER NUMBER
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2134

NOTIFICATION DATE	DELIVERY MODE
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10/24/2007

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com  
uspto@dlemail.itg.ti.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/806,963	<b>Applicant(s)</b> GOSS, STEVEN C.	
	<b>Examiner</b> William S. Powers	<b>Art Unit</b> 2134	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Information Disclosure Statement*

1. No Information Disclosure Statement was submitted with the application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The Examiner has stated the below column and line numbers as examples. All columns and line numbers in the reference and the figures are relevant material and Applicant should be taken the entire reference into consideration upon the reply to this Office Action.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,825,878 to Takahashi et al. (hereinafter Takahashi).

As to claims 1 and 8, Takahashi teaches:

a. A key register located within said SEE and coupled to said secure memory to receive a cryptographic key therefrom (key register with cryptographic keys stored within the key register) (Takahashi, column 5, lines 34-50 and figure 2).

b. Data input and output registers located outside of said SEE and coupled to said key register to allow said cryptographic key to be applied to input data arriving via said data input register to yield output data via said data output register (input and output is controlled by the memory controller the accesses the external memory) (Takahashi, Abstract, figure 1, column 3, lines 6-20 and column 6, lines 14-35).

As to claims 2, 9 and 16, Takahashi teaches a secure data bus coupling said key register and said secure memory is isolated from external pins of said SoC (the integrated chip is constructed to prevent access to the internal buses and connectors of the chip) (Takahashi, column 2, lines 40-48 and figure 1).

As to claims 3, 10 and 17, Takahashi teaches a cryptographic block coupled to said key register and said data input and output registers consists of a Data Encryption Standard (DES) block (uses the DES algorithm) (Takahashi, column 5, lines 16-22).

As to claim 4, 11 and 18, Takahashi teaches said key register is a write-only register and writeable only when a central processing unit of said SoC is in a

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secure state (write request must be initiated by the internal OS) (Takahashi, column 6, lines 14-35).

As to claims 5, 12 and 19, Takahashi teaches a data bus coupled to said input and output registers is further coupled to external pins of said SoC (memory controller of the integrated chip is connected to the external memory, which is the only access to elements not on the chip) (Takahashi, column 6, lines 14-35 and figure 1).

As to claims 6, 13 and 20, Takahashi teaches a central processing unit mediates movement of said input data and said output data between said input and output registers and memory external to said SoC (CPU core and DMA control the inputting, outputting, encryption and decryption of data) (Takahashi, column 4, lines 45-58 and figures 2 and 3).

As to claims 7,14, Takahashi teaches said secure memory comprises secure read-only memory and secure static random access memory (integrated chip consists of SRAM and ROM that is located within the secure environment of the integrated chip) (Takahashi, figure 1, column 3, lines 6-20 and column 6, lines 43-47).

As to claim 15, Takahashi teaches:

- a. A central processing unit (CPU) (Takahashi, column 2, lines 49-53 and figure 1).
- b. Secure read only memory (integrated chip consists ROM that is located within the secure environment of the integrated chip) (Takahashi, column 6, lines 43-47).
- c. Secure static random access memory, said CPU and said secure memory configured to provide a secure execution environment (integrated chip consists of SRAM that is located within the secure environment of the integrated chip) (Takahashi, figure 1, column 3, lines 6-20).
- d. A key register located within said SEE and coupled to said secure memory to receive a cryptographic key therefrom (key register with cryptographic keys stored within the key register) (Takahashi, column 5, lines 34-50 and figure 2).
- e. Data input and output registers located outside of said SEE and coupled to said key register to allow said cryptographic key to be applied to input data arriving via said data input register to yield output data via said data output register (input and output is controlled by the memory controller the accesses the external memory) (Takahashi, Abstract, figure 1, column 3, lines 6-20 and column 6, lines 14-35).

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**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William S. Powers whose telephone number is 751 272 8573. The examiner can normally be reached on m-f 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on 571 272 3811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
10/16/2007

  
KAMBIZ ZAND  
SUPERVISORY PATENT EXAMINER

William S. Powers  
Examiner  
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